



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,232	10/23/2006	Tae-Kyung Yoo	718936.17	6109
27128	7590	06/24/2010	EXAMINER	
HUSCH BLACKWELL SANDERS LLP			WEBB, VERNON P	
190 Carondelet Plaza				
Suite 600			ART UNIT	PAPER NUMBER
ST. LOUIS, MO 63105			2811	
			NOTIFICATION DATE	DELIVERY MODE
			06/24/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pto-sl@huschblackwell.com

Office Action Summary	Application No.	Applicant(s)	
	10/599,232	YOO ET AL.	
	Examiner	Art Unit	
	VERNON P. WEBB	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 September 2006.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 22 September 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>09/22/2006 and 03/04/2009</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Status of Application

1. This office action is in response to the filing of the application papers on 22 September 2006. Claims 1-20 are pending in this application.

Foreign Priority

2. Acknowledgement is made that the certified copy of the foreign priority document has been received.

Information Disclosure Statement

3. Acknowledgement is made that the information disclosure statements filed 9/22/2006 and 03/04/2009 has been received and considered by the examiner. If the applicant is aware of any prior art or any other co-pending applications not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: III-Nitride Compound Semiconductor Light Emitting Device with Carbon-Compound Material Formed Within.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 5, 7, 9, 12, 13, 16 and 7 rejected under 35 U.S.C. 102(b) as being anticipated by Kamimura et al. (J.P. Pub. Application 10-084159).

7. Claim 1, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device including an n- type III-nitride semiconductor layer (item 103), an active layer (items 105) made of III-nitride semiconductor and deposited over the n-type III-nitride semiconductor layer (item 103), a p-type III-nitride semiconductor layer (item 106) deposited over the active layer (items 105) made of III-nitride semiconductor, and a p-side electrode (item 114) deposited over the p- type III-nitride semiconductor layer (106) (pgs. 3-4, paragraphs [0014-0024]; Fig. 1), the light emitting device comprising:

- a first layer (item 109) composed of a carbon-containing compound layer, the first layer (item 109) interposed between the p-type III-nitride semiconductor layer (item 106) and the p-side electrode (item 114) and grown on the p-type III -nitride semiconductor layer (item 106) (pg. 5, paragraphs [0028] and [0030]; Fig. 1).
- and a second layer (item 107) composed of a III-nitride semiconductor layer (pg. 4, paragraph [0021]; Fig. 1),

8. Kamimura et al. discloses a semiconductor structure, the limitation of “*wherein the second layer grown after the first layer is grown*”, this is considered a product-by-process claim. “Even though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself (See **MPEP 2113**). The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a

different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

9. Regarding claim 3, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 1, wherein the first layer (item 109) is one selected from the group consisting of silicon carbide (Si_aC_b ; $a,b \neq 0$), silicon carbon nitride ($Si_cC_dN_e$; $c,d,e \neq 0$) and 20 carbon nitride (C_fN_g ; $f,g \neq 0$) (pg. 4, paragraph [0023]; Fig. 1).

10. Regarding claim 5, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the second layer (item 107) is a p-type III-nitride semiconductor layer (pg. 4, paragraph [0021]; Fig. 1).

11. Regarding claim 7, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the first layer (item 109) is in a thickness of 5Å to 1000Å (pg. 4, paragraph [0023]; Fig. 1).

12. Regarding claim 9, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claims 3, wherein the first layer (item 109) is a p-type carbon-containing compound layer (pg. 4, paragraph [0023]; Fig. 1).

13. Regarding claim 12, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the first layer (item 109) is formed as a uniform layer (pg. 4, paragraph [0023]; Fig. 1).

14. Regarding claim 13, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the

second layer (item 107) is in a thickness of 100Å to 5000Å (pgs. 3-4, paragraph [0020]; Fig. 1).

15. Regarding claim 16, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the p-side electrode (item 113/114) is made of any one selected from the group consisting of nickel, gold, silver, chrome, titanium, platinum, palladium, rhodium, iridium, aluminum, tin, ITO, indium, tantalum, copper, cobalt, iron, ruthenium, zirconium, tungsten, and molybdenum (pg. 5, paragraph [0028]; Fig. 1).

16. Regarding claim 17, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the silicon source for growing the first layer (item 109) is any one selected from the group consisting of SiH_4 , Si_2H_6 , and DTBSi, the carbon source for growing the first layer (item 109) is any one selected from the group consisting of CH_4 , C_2H_4 , and CBr_4 , and the nitrogen source for growing the first layer is any one selected from the group consisting of NH_3 , and Hydrazine-based source material (pg. 4, paragraph [0023]; Fig. 1).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. (J.P. Pub. Application 10-084159).

20. Regarding claim 8, Kamimura et al. discloses the claimed invention except for wherein the growth temperature of the first layer (item 109) is 500 °C to 1,100 °C. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the growth temperature of the first layer is 500 °C to 1,100 °C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller* 105 USPQ 233 (CCPA 1955).

21. Regarding claim 10, Kamimura et al. discloses the claimed invention except for wherein the first layer is a n-type carbon-containing compound layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the first layer is a n-type carbon-containing compound layer; since it has been held to be within the general skill of a worker in the art to select a

known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

22. Regarding claim 11, Kamimura et al. discloses the claimed invention except for wherein the first layer is formed as a nonuniform layer. It would have been an obvious matter of design choice to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al. wherein the first layer is formed as a nonuniform layer, since such a modification would have involved a mere change in the size of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art *In re Dailey*, 357 USPQ 47 (CCPA 1966).

23. Claims 2, 4, 6, 14, 15, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. (J.P. Pub. Application 10-084159) as applied to claim 1 above, and further in view of Sugawara (U.S. Pub. Application 2004/0119082 A1).

24. Regarding claim 2, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 1.

25. Kamimura et al. does not disclose a III-nitride compound semiconductor light emitting device, wherein the second layer is composed of a plurality of island.

26. However Sugawara discloses a III-nitride compound semiconductor light emitting device Kamimura et al., wherein the second layer (item 17) is composed of a plurality of islands (pg 3, paragraphs [0052] and [0060]; Figs. 2-7).

27. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the second layer is composed of a plurality of island as disclosed by Sugawara with at least the motivation of increasing its contact area with

the electrode of the device and thus provides a sufficiently low electric contact resistance (pg. 2, paragraph [0024]).

28. Regarding claim 4, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 3, wherein the n-type III-nitride semiconductor layer (item 103), the active layer (item 105) made of III-nitride semiconductor, the p-type III-nitride semiconductor layer (item 106), and the second layer (item 109) is composed of $\text{Al}(x)\text{Ga}(y)\text{In}(1-x-y)\text{N}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) (pg. 3, paragraphs [0017] and [0019]; pg. 4, paragraph [0023]; Fig. 1)

29. Kamimura et al. does not disclose a III-nitride compound semiconductor light emitting device, wherein the second layer is grown in a form of a plurality of islands due to different material characteristics between the first layer and the second layer.

30. However Sugawara discloses a III-nitride compound semiconductor light emitting device, wherein the second layer (item 17) is grown in a form of a plurality of islands due to different material characteristics between the first layer (item 16) and the second layer (item 17) (pg. 3, paragraphs [0050-0053]; Figs. 2-7).

31. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the second layer is grown in a form of a plurality of islands due to different material characteristics between the first layer and the second layer as disclosed by Sugawara with at least the motivation of increasing its contact area with the electrode of the device and thus provides a sufficiently low electric contact resistance (pg. 2, paragraph [0024]).

32. Regarding claim 6, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 4, wherein the second layer (item 109) is composed of $\text{Al}(x)\text{Ga}(y)\text{In}(1-x-y)\text{N}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) (pg. 4. paragraph [0023]; Fig. 1).

33. Regarding claim 14, Kamimura et al. as modified by Sugawara discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 6, further comprising: a third layer (item 15) made of $\text{Al}(x)\text{Ga}(y)\text{In}(1-x-y)\text{N}$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) (pg. 3. paragraph [0049]; Figs. 2-7)

34. Kamimura et al. discloses a semiconductor structure, the limitation of “*comprising a third layer... grown after the second layer is grown*”, this is considered a product-by-process claim. “Even though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself (See **MPEP 2113**). The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

35. Regarding claim 18, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device comprising:

- a substrate (item 101) (pg. 3, paragraph [0014]; Fig. 1);
- a buffer layer (item 102) deposited on the substrate (item 101) (pg. 3, paragraph [0016]; Fig. 1);

Art Unit: 2811

- an n-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) layer (item 103) deposited on the buffer layer (item 102) (pg. 3, paragraph [0017]; Fig. 1);
- an $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) active layer (item 105) deposited on the n-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) layer (item 103) (pg. 3, paragraph [0019]; Fig. 1);
- an-p-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) layer (item 106) deposited on the $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) active layer (item 105) (pgs. 3-4, paragraph [0020]; Fig. 1)
- a first layer (item 109) made of one selected from the group consisting of silicon (Si_aC_b ; $a,b \neq 0$), silicon carbon nitride ($Si_cC_dN_e$; $c,d,e \neq 0$) and carbon nitride (C_fN_g ; $f,g \neq 0$), and grown on the p-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) layer (item 106) (pg. 4, paragraph [0023]; Fig. 1);
- a second layer (item 107) made of p-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) (pg. 4, paragraph [0021]; Fig. 1),
- a p-side electrode (item 113/114) deposited on the second layer (item 107) (pg. 5, paragraph [0028]; Fig. 1)
- an n-side electrode (item 111/112) deposited on the n-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1, 0 \leq y \leq 1, 0 \leq x+y \leq 1$) layer (item 103) (pg. 5, paragraph [0028]; Fig. 1)

36. Kamimura et al. discloses a semiconductor structure, the limitation of “*wherein the second layer grown after the first layer is grown*”, this is considered a product-by-process claim. “Even though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself (See **MPEP 2113**). The patentability of a product does not depend on its method of production. If the

product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

37. Additionally Kamimura et al. does not disclose a III-nitride compound semiconductor light emitting device, wherein the second layer is composed of a plurality of island for increasing external quantum efficiency.

38. However Sugawara discloses a III-nitride compound semiconductor light emitting device Kamimura et al., wherein the second layer (item 17) is composed of a plurality of islands for increasing external quantum efficiency (pg 3, paragraphs [0052] and [0060]; Figs. 2-7).

39. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the second layer is composed of a plurality of island for increasing external quantum efficiency as disclosed by Sugawara with at least the motivation of increasing its contact area with the electrode of the device and thus provides a sufficiently low electric contact resistance (pg. 2, paragraph [0024]).

40. Regarding claim 19, Kamimura et al. discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 18, wherein the - p-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) layer (item 106) and the second layer (item 107) made of p-type $Al(x)Ga(y)In(1-x-y)N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x+y \leq 1$) are made of GaN (pgs. 3-4, paragraphs [0020-0021]; Fig. 1)

41. Regarding claim 20, Kamimura et al. as modified by Sugawara discloses a III-nitride compound semiconductor light emitting device as described in reference to claim 18, wherein the light emitting device (item 21) is a light emitting diode (pg.4, paragraph [0070]; Fig. 2)

42. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a III-nitride compound semiconductor light emitting device as disclosed by Kamimura et al., wherein the light emitting device is a light emitting diode as disclosed by Sugawara as this a form of light emitting device is commonly known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VERNON P. WEBB whose telephone number is (571)270-3332. The examiner can normally be reached on Monday through Friday, 7:30 am to 5 pm, Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1760. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/V. Parris Webb/
Examiner, Art Unit 2811

/Hung Vu/
Primary Examiner, Art Unit 2811